TEMIC Semiconductors

TN0601L, VN0606L/M, VN66AFD

N-Channel Enhancement-Mode MOS Transistors

Product Summary

Part Number	$V_{(BR)DSS}$ Min (V)	$r_{DS(on)}$ Max (Ω)	$V_{GS(th)}$ (V)	I_D (A)
TN0601L	60	1.8 @ V_{GS} = 10 V	0.5 to 2	0.47
VN0606L		3 @ V_{GS} = 10 V	0.8 to 2	0.33
VN0606M		3 @ V_{GS} = 10 V	0.8 to 2	0.39
VN66AFD		3 @ V_{GS} = 10 V	0.8 to 2.5	1.46

Features

- Low On-Resistance: 1.2 Ω
- Low Threshold: <1.6 V
- Low Input Capacitance: 35 pF
- Fast Switching Speed: 9 ns
- Low Input and Output Leakage

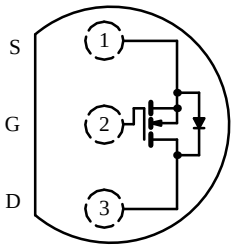
Benefits

- Low Offset Voltage
- Low-Voltage Operation
- Easily Driven Without Buffer
- High-Speed Circuits
- Low Error Voltage

Applications

- Direct Logic-Level Interface: TTL/CMOS
- Drivers: Relays, Solenoids, Lamps, Hammers, Displays, Memories, Transistors, etc.
- Battery Operated Systems
- Solid-State Relays

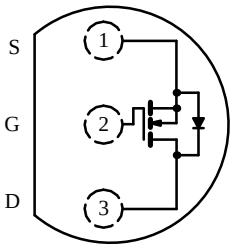
TO-226AA
(TO-92)



Top View

TN0610L
VN0606L

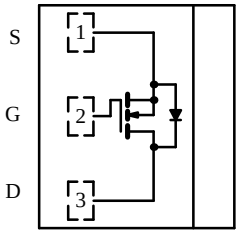
TO-237
(Tab Drain)



Top View

VN0606M

TO-220SD
(Tab Drain)



Top View

VN66AFD

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	TN0601L	VN0606L	VN0606M	VN66AFD[b]	Unit
Drain-Source Voltage		V_{DS}	60	60	60	60	V
Gate-Source Voltage		V_{GS}	±20	±30	±30	±30	
Continuous Drain Current (T_J = 150°C)	T_A= 25°C	I_D	0.47	0.33	0.39	1.46	A
	T_A= 100°C		0.29	0.21	0.25	0.92	
Pulsed Drain Current[a]		I_{DM}	1.5	1.6	2	3	
Power Dissipation	T_A= 25°C	P_D	0.8	0.8	1.0	15	W
	T_A= 100°C		0.32	0.32	0.4	6	
Maximum Junction-to-Ambient		R_{thJA}	156	156	125		°C/W
Maximum Junction-to-Case		R_{thJC}				8.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150				°C

Notes
a. Pulse width limited by maximum junction temperature.
b. Reference case for all temperature testing.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70201.

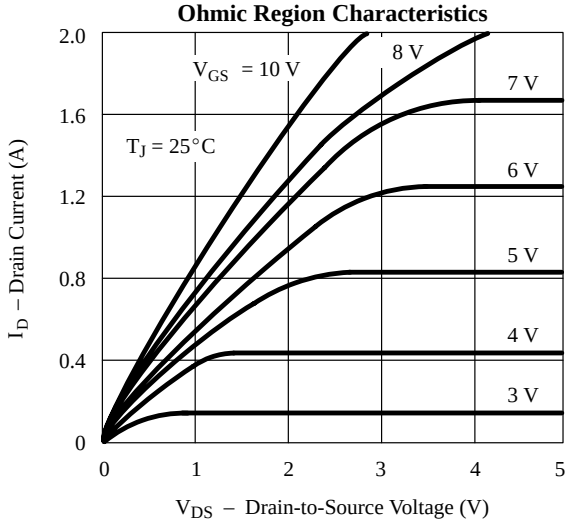
Specifications[a]

Parameter	Symbol	Test Conditions	Typ[b]	Limits TN0601L Min	TN0601L Max	VN0606L VN0606M Min	VN0606L VN0606M Max	VN66AFD Min	VN66AFD Max	Unit
Static										
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 10 µA	70	60		60		60		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 0.25 mA	1.6	0.5	2					
		V_{DS} = V_{GS}, I_D = 1 mA	1.7			0.8	2	0.8	2.5	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±30 V					±100		±100	nA
		T_C = 125°C							±500	
		V_{DS} = 0 V, V_{GS} = ±20 V			±10					
Zero Gate VoltageDrain Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V					10			µA
		T_J = 125°C					500			
		V_{DS} = 48 V, V_{GS} = 0 V			1				1	
		T_J = 125°C			100					
		T_C = 125°C							10	
On-State Drain Current[c]	$I_{D(on)}$	V_{DS} = 10 V, V_{GS} = 4.5 V	0.5	0.25						A
		V_{DS} = 10 V, V_{GS} = 10 V	2.4	1		1.5		1.5		
Drain-Source On-Resistance[c]	$r_{DS(on)}$	V_{GS} = 3.5 V, I_D = 0.04 A	4		5					Ω
		V_{GS} = 4.5 V, I_D = 0.25 A	2		3					
		T_J = 125°C	3.8		6					
		V_{GS} = 5 V, I_D = 0.3 A	2.3						5	
		V_{GS} = 10 V, I_D = 0.5 A	1.2				3			
		T_J = 125°C	2.3				6			
		V_{GS} = 10 V, I_D = 1 A	1.3		1.8				3	
		T_C = 125°C	2.5						6	
Forward Transconductance[c]	g_{fs}	V_{DS} = 10 V, I_D = 0.5 A	350	200		170		170		mS
Common Source Output Conductance[c]	g_{os}	V_{DS} = 10 V, I_D = 0.1 A	0.3							
Dynamic										
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	35		60		50		50	pF
Output Capacitance	C_{oss}		25		50		40		40	
Reverse Transfer Capacitance	C_{rss}		6		10		10		10	
Switching[d]										
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 23 Ω, I_D ≅ 1 A, V_{GEN} = 10 V, R_G = 25 Ω	8		15		10		15	ns
Turn-Off Time	t_{OFF}		9		15		10		15	

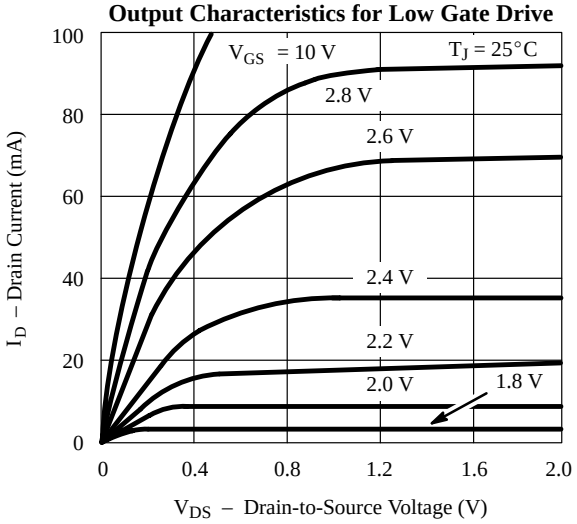
Notes
a. T_A = 25°C unless otherwise noted. VNDQ06
b. For DESIGN AID ONLY, not subject to production testing.
c. Pulse test: PW ≤ 300 µs duty cycle ≤ 2%.
d. Switching time is essentially independent of operating temperature.

Typical Characteristics (25°C Unless Otherwise Noted)

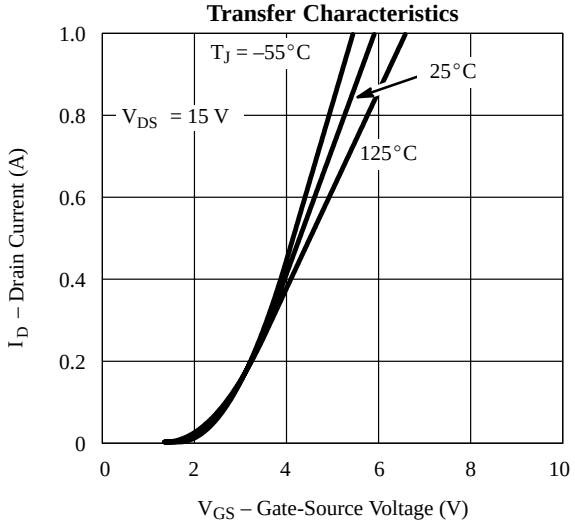
Ohmic Region Characteristics



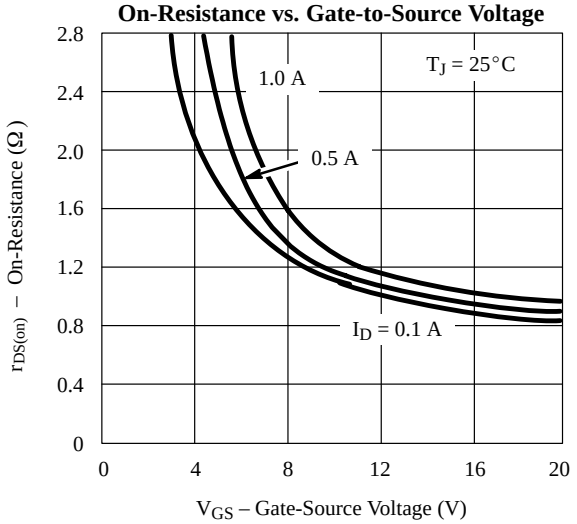
Output Characteristics for Low Gate Drive



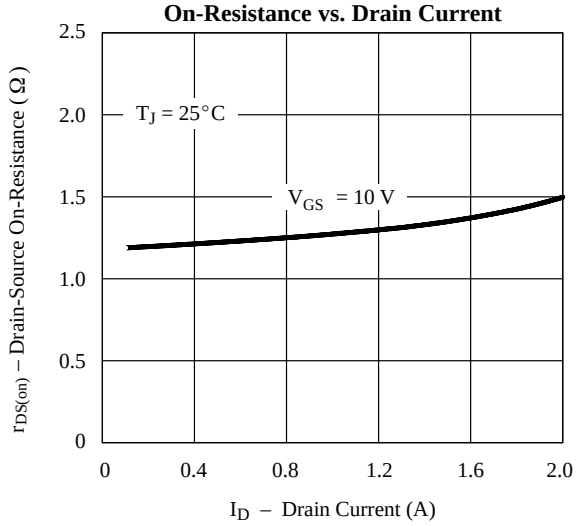
Transfer Characteristics



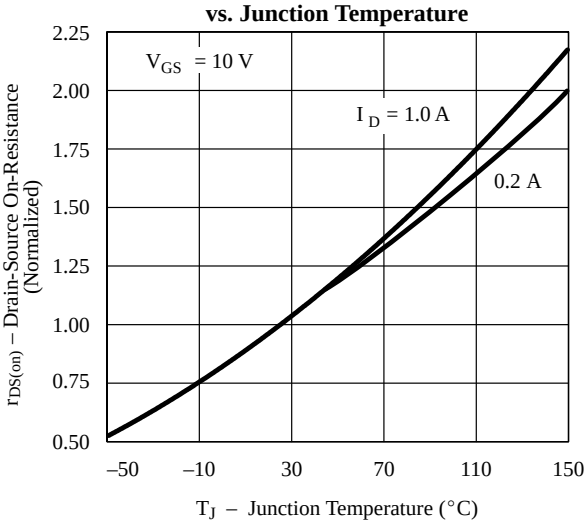
On-Resistance vs. Gate-to-Source Voltage



On-Resistance vs. Drain Current

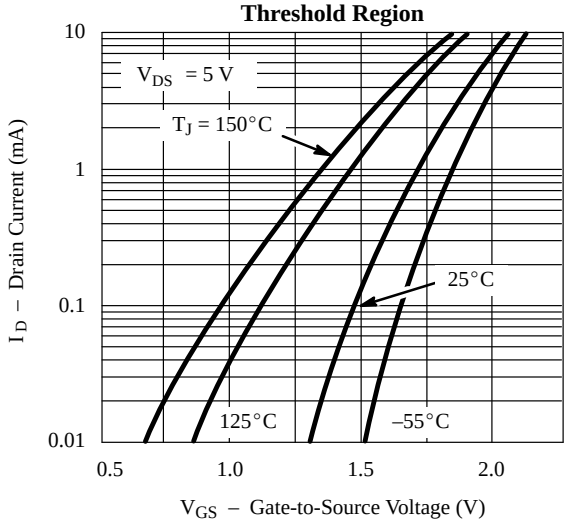


Normalized On-Resistance vs. Junction Temperature

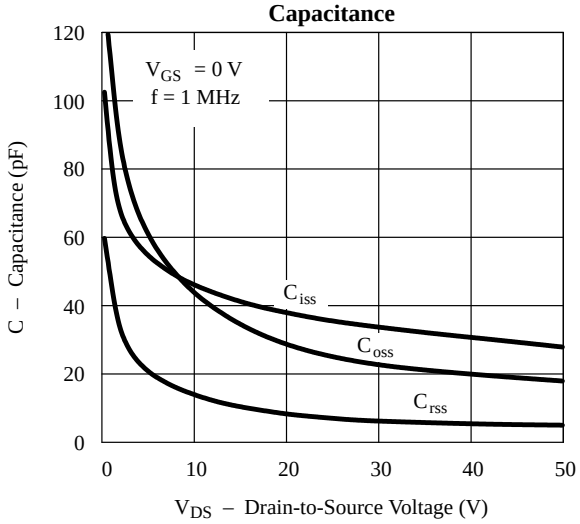


Typical Characteristics (25°C Unless Otherwise Noted)

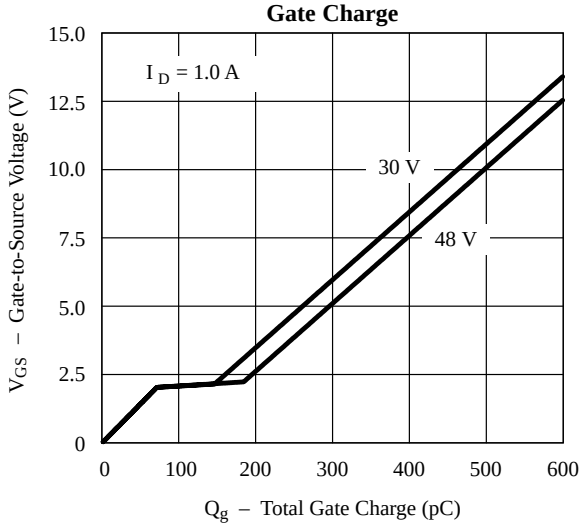
Threshold Region



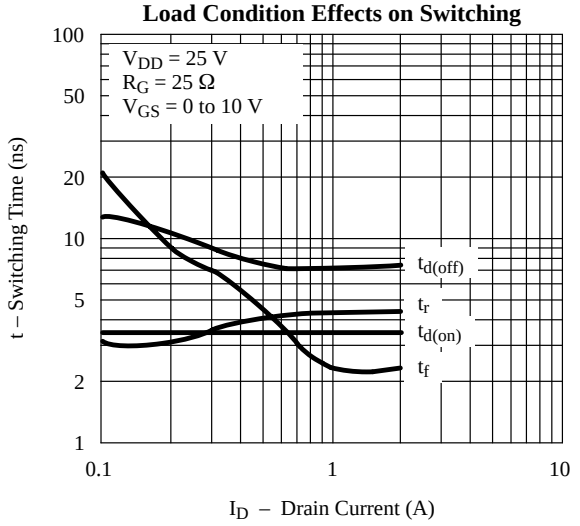
Capacitance



Gate Charge



Load Condition Effects on Switching



Normalized Effective Transient Thermal Impedance, Junction-to-Ambient (TO-226AA, TO-237)